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10/064,454	07/17/2002	Kuang-Kai Kuo	8327-US-PA	5796

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	3

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,454	KUO ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings filed on 17 July 2002 have been approved by the Examiner.

Specification

3. The disclosure is objected to because of the following informalities:

The references to Figs. 2 and 3 in the specification appear to be incorrect. The specification refers to Fig. 2 as being a transmission format (Page 6, paragraph 20) whereas Fig. 2 depicts a timing diagram. The specification refers to Fig. 3 as being a timing diagram (Page 7, paragraph 21) whereas Fig. 3 depicts a transmission format.

It is suggested that the references to Figs. 2 and 3 be interchanged. The specification will be interpreted in light of this suggestion.

Appropriate correction of the above noted deficiencies is required.

Claim Objections

4. Claims 1-11 are objected to because of the following informalities:

The parent claim references in claims 5,6,9 and 10 are not in accordance with 37 CFR 1.75 which requires that dependent claims refer back to another claim in the application. Claims 5 and 9 contain forward references to claims 6 and 10, respectively. Claims 6 and 10 contain references to themselves.

For the purposes of examination, claims 5 and 6 will both be treated as dependent upon claim 1. Likewise, claims 9 and 10 will both be treated as dependent upon claim 8.

The phrase "said write address of said memory-write commands" (Claim 1, lines 13 and 18) makes improper use of the plural and singular word forms. As written, a single write address is associated with a plurality of commands. It is suggested that this phrase be replaced by the phrase "each said write address of said memory-write commands". The claim(s) will be interpreted in light of this suggestion.

The phrase "until said memory-write command inside said memory-write command queue" (Claim 1, lines 23-24) is improper because there is no action, event or time following the word "until". Furthermore, the phrase "said memory-write command" is improper because a singular memory-write command has not been recited previously in the claim.

It is suggested that the word "executes" be appended to the end of this phrase, and the phrase "said memory-write command" be replaced by the phrase "the memory write command with identical address bits". The claim(s) will be interpreted in light of this suggestion.

The phrase "said grant execution is set only after said memory-write command inside memory-write command queue" (Claim 2, lines 19-20) is improper because there is no action, event or time following the word "after". Furthermore, the phrase "said memory-write command" is improper because a singular memory-write command has not been recited previously in the claim.

It is suggested that the word "executes" be appended to the end of this phrase, and the phrase "said memory-write command" be replaced by the phrase "the memory write command with identical address bits". The claim(s) will be interpreted in light of this suggestion.

Claims 4 and 9 omit punctuation so that their meaning is unclear. For example, the claims may be interpreted such that the rising edge is defined as a bit time period and that the falling edge is defined as two bit time periods. However, the specification teaches that each edge is defined as a single bit time (Page 4, paragraph 9). Furthermore, it appears that a verb has been omitted from line 3 of claim 4, and additional wording has been erroneously deleted from line 3 of claim 9. It is suggested that a comma be inserted prior to the word "and" in line 2 of claims 4 and 9, the word "are" be inserted prior to the word "required" in line 3 of claim 4, and that a space and the phrase "are required" be inserted following the word "periods" in claim 9. The claim(s) will be interpreted in light of this suggestion.

Claim 8 contains two consecutive commas in line 4. One comma should be deleted.

The phrase "said first section read address" (Claim 8, line 6) is improper because a first section read address has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a first section read address". The claim(s) will be interpreted in light of this suggestion.

The phrase "said write address of said memory-write commands" (Claim 8, lines 7-8 and 13-14) makes improper use of the plural and singular word forms. As written, a single write address is associated with a plurality of command. It is suggested that this phrase be replaced by the phrase "each said write address of said memory-write commands". The claim(s) will be interpreted in light of this suggestion.

The phrase "said execution" (Claim 8, line 10) is improper because an execution has not been previously recited in the claims. It is suggested that the word "said" be deleted. The claim(s) will be interpreted in light of this suggestion.

The phrase "said memory read command" (Claim 8, lines 10-11) is improper because a memory read command has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a memory read command associated with the first section read address". The claim(s) will be interpreted in light of this suggestion.

The phrase "to receive said second section read address transmitted through said system bus" (Claim 8, lines 11-12) is unclear and appears to be a fragment of a separate method step. Furthermore, it contains an improper reference to a second section read address that has not been previously recited in the claims.

It is suggested that a semicolon be placed after the word "command" in line 11, and the cited phrase be placed on a new line, modified to read "receiving a second section read address transmitted through said system bus" and followed by a semicolon.

The word "indicating" (Claim 8, lines 10 and 16) makes improper use of the inflected form. It is suggested that this word be replaced by the word "indicates". The claim(s) will be interpreted in light of this suggestion.

The phrase "said presence of identical bits" (Claim 8, line 18) is improper because a presence of identical bits has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a presence of identical bits". The claim(s) will be interpreted in light of this suggestion.

The phrase "said clock signal" (Claim 9, lines 1-2) is improper because a clock signal has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a clock signal". The claim(s) will be interpreted in light of this suggestion.

The phrase "the memory read command queue" (Claim 10, line 2) is improper because a memory read command queue has not been previously recited in the claims. It is suggested that this phrase be replaced by the phrase "a memory read command queue". The claim(s) will be interpreted in light of this suggestion.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction of the above noted deficiencies is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 7 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The North Bridge chip and main board recited in claim 7 are not specified, defined or described in the specification.

Claim 11 appears to describe an interlock between the arrival of subsequent memory read commands and execution of previously received read commands. It is unclear from the specification how these are related. For example, it is unclear whether there may be zero or more bit time units between successive memory read commands, or whether they may be intermixed with memory write commands. As stated, the claim appears to contradict the advantages set forth in the disclosure. Specifically, making execution of a memory read command depend upon the arrival of a subsequent memory read command may add unnecessary delay, whereas the stated objective of the invention is to accelerate memory access.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 7 recites the limitation "said North Bridge chip of a main board" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 11 recites the limitations "said memory-write command" in lines 2-3, and "the first bit period" and "said next read command" in lines 5. A singular memory-write command, first bit-period and next read command have not been previously recited in the claims. There is insufficient antecedent basis for these limitations in the claim.

Prior art has not been applied to claims 7 and 11 due to the above noted deficiencies.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 5-6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379) in view of Mills (US 5,497,355) and Pollak (US 6,618,724).

As in claims 1 and 5-6, Becker describes a memory control system coupled to a system bus (Figs. 1 and 5a, elements 12 and 22; column 3, lines 11-16 and 30-33) and having a clock line (Figs. 3a-3c, element labeled "CLK"; column 6, lines 28-38), where the memory control system comprises:

a memory write command queue for holding a plurality of memory write commands, wherein each said memory write command has an address (Fig. 5a, elements 90 and 92; column 8, lines 53-57);

wherein the memory control system receives a read address of a read command (i.e. a memory read operation) according to a clock signal (Fig. 1; column 4, lines 31-36; Figs. 3b-3c; column 6, lines 43-62; column 8, lines 1-17);

a memory request organizer function wherein the read address is compared with the write address of each memory write command in the memory write command queue, and if the comparison indicates the presence of identical bits, the execution of the memory read command is delayed until the matching memory write commands in the memory write command queue execute (Column 9, lines 1-9; column 12, lines 19-35); and

wherein if the comparison indicates a difference, execution of the memory read command is permitted (Column 12, lines 63-66).

Becker does not teach that the read address is received sequentially by a bus interface unit as a first and second section, and that the first and second sections are output concurrently, as required by claims 1 and 5-6.

Mills teaches an address demultiplexer coupled to a memory request bus (i.e. a bus interface unit) where an address is received sequentially as a row address (i.e. first section) and column address (i.e. second section), and the row and column addresses are output concurrently (Fig. 5, column 13, lines 3-13). Mills teaches that this arrangement allows synchronous address latching circuitry to work with multiplexed addresses such as those occurring in dynamic random access memories (Column 12, lines 57-60).

Regarding claims 1 and 5-6, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address demultiplexing arrangement taught by

Mills, in the system of Becker, in order to allow synchronous address latching circuitry to work with multiplexed addresses as taught by Mills.

The combination of Becker and Mills does not teach a two-step comparison algorithm where the first section read address is first compared, and the second section read address is compared if the first section read address indicates a match, as required by claims 1 and 5-6.

Pollak teaches a string comparison algorithm where characters comprising identical bit portions of two strings are compared such that if the first characters match (i.e. first section), the second characters (i.e. second section) are subsequently compared, but if the first characters do not match, the comparison is terminated and execution of a controlling process continues (Fig. 2, column 4, lines 18-39). It may be understood from the teaching of Pollak that by stopping the comparison after the first mismatch is found, the time required to compare the strings is less than if the entire strings were compared (Column 1, line 66 to column 2, line 4).

Regarding claims 1and 5-6, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to compare the read address as a series of subsequent comparisons on a first and second section of the read address as in the comparison algorithm taught by Pollak, in the system made obvious by the combined teachings of Becker and Mills, in order to reduce the time required to make the comparison as taught by Pollak.

Regarding claims 5-6, although the combination of Becker, Mills and Pollak does not teach that when comparing the first and second sections of the read and write addresses, the first section of the address includes bits 12 to 31, and that the second section of the address includes bits 6 to 11, such limitations are merely a matter of design choice and would have been obvious in the system of Becker, Mills and Pollak. Becker, Mills and Pollak teach a comparison made between the first sections of a read and write address, and a comparison made between the second sections of a read and write address. The limitations in claims 5-6 of the instant application do not define a patentably distinct invention over Becker, Mills and Pollak since both are directed toward comparing addresses that are divided into two distinct portions. The particular assignment of bit ranges to these portions is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to assign bits 12 to 31 as the first section of the address, and to assign bits 6 to 11 as the second section of the address would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant.

Method claim 8 is rejected using the same rationale as for the rejection of claim 1 above.

As in claim 10, Becker teaches that a memory read command may be output directly via a fast path, and that a memory read command may alternatively be transferred to a memory read command queue (Fig. 5a, elements 94, 152 and "FAST"; column 15, line 50 to column 16, line 2).

12. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 1 above, and further in view of Mann (US 5,954,813).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as above.

The combination of Becker, Mills and Pollak does not teach the following limitations required by claims 2-3:

a first and second compare unit coupled to the bus interface unit for receiving the first and second section read addresses, respectively, and comparing the first and second section read addresses to the identical bit portions of each write address of the memory write commands inside the memory write command queue, and outputting a first and second comparison signal; and

a grant decision unit coupled to the first and second comparison units, wherein a grant execution signal is set if either compare unit indicates a difference, otherwise the grant execution signal is set only after the memory write command with identical address bits executes.

Referring to the rationale for the rejection of claim 1, it is noted that Becker, Mills and Pollak teach the comparison of a read address against the write addresses in a memory write command queue, and granting execution of the read command if there is no match, and delaying execution of the read command until the matching write command executes if there is a match.

However, Becker, Mills and Pollak do not teach the specific configuration of the comparison function enumerated above, particularly the use of two compare units and a grant decision unit.

Mann teaches the comparison of an address divided into a first and second section against a stored address using two comparators (i.e. compare units), where a control unit (i.e. grant decision unit) receives the results of the comparison from each comparator and outputs a signal (i.e. grant execution signal) to allow the continued execution of a process if the addresses do not match, and halt execution of a process if the addresses match (Fig. 3; column 3, lines 47-55; column 6, lines 11-52).

Regarding claims 2-3, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address comparison configuration taught by Mann to execute the address comparison function in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the similarity in the nature of the problem to be solved which would have been recognized by one of ordinary skill in the art at the time of the invention.

Regarding claim 3, the rationale derived from Becker in the rejection of claim 10 above is incorporated herein for the teaching that a memory read command may be output directly via a fast path, and that a memory read command may alternatively be transferred to a memory read command queue.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 1 above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as above.

The combination of Becker, Mills and Pollak does not teach that transfer of the first section read address requires two bit times, where a rising edge and a falling edge of the clock are both defined as a bit time, as required by claim 4.

APA describes a system bus defined by AMD Corporation where each rising and falling edge of the clock signal is defined to be a single bit time unit and the first section read address is transmitted in two bit time units (Page 4, paragraph 9).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to define each rising and falling edge of the clock signal to be a single bit time unit, and to require two bit time units to transfer the first section read address, in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the applicant's own admitted prior art.

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 8 above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 8 as above.

The combination of Becker, Mills and Pollak does not teach that transfer of the first section read address requires two bit times, where a rising edge and a falling edge of the clock are both defined as a bit time, as required by claim 9.

The rationale set forth in the rejection of claim 4 is applied herein for the rejection of claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JMR

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER